CLAIMS

What is claimed is:

1. A high frequency power amplifier having a plurality of amplifying systems, each of said amplifying systems comprising:

an input terminal to which a signal to be amplified is supplied;

an output terminal;

a bias terminal;

a plurality of amplifying stages which are sequentially cascaded between said input terminal and output terminal; and

a bias circuit connected to said bias terminal and each of said amplifying stages to apply a bias potential to said amplifying stage, said amplifying stage including a control terminal for receiving an input signal and said bias potential supplied to the stage and a first terminal for transmitting an output signal of the stage, a first amplifying systems and a second amplifying stage of each of said amplifying stages being monolithically formed on a single semiconductor chip, a part of bias resistors included in the bias circuits of said first amplifying stage and second amplifying stage being monolithically formed on said semiconductor chip.

2. A high frequency power amplifier according to Claim 1, wherein said control terminals and first terminals of said

first amplifying stage and second amplifying stage on a surface of said semiconductor chip are alternately provided in the same direction.

3. A high frequency power amplifier according to Claim 1, wherein a wire that is connected to the control terminal of said second amplifying stage provided on a surface of said semiconductor chip and a wire connected to the first terminal of said second amplifying stage extend in directions crossing each other.

4. A high frequency power amplifier according to Claim 3, wherein the wire that is connected to the control terminal of said second amplifying stage and the wire connected to the first terminal of said second amplifying stage extend in directions orthogonal to each other.

5. A high frequency power amplifier according to Claim 1, wherein a bias resistance ratio of the first amplifying stage of each of said amplifying stages or bias resistance ratios of the first amplifying systems and second amplifying stage can be adjusted.

6. A high frequency power amplifier according to Claim 5, wherein the bias resistance ratio of the first amplifying stage

of each of said amplifying systems or the bias resistance ratios of the first amplifying stage and second amplifying stage are adjusted by selecting connecting positions of electrical connectors that connect the plurality of bias resistors formed on the surface of said semiconductor chip, the choice including no connection with the electrical connectors.

7. A high frequency power amplifier according to Claim 1, wherein a bias control circuit is connected to said bias terminal and wherein terminals of the bias control circuit for output to said first amplifying stage and second amplifying stage are connected to the control terminals of said first amplifying stage and second amplifying stage.

8. A high frequency power amplifier according to Claim 1, wherein a transistor that serves as the final amplifying stage of each of said amplifying systems is any of a Si-MOSFET, SiGe-FET, GaAs-MESFET, HEMT, and hetero-junction type bipolar transistor.

9. A wireless communication apparatus comprising a high frequency power amplifier according to Claim 1.

10. A high frequency power amplifier according to Claim 1, wherein a transistor included in each of said plurality of

amplifying stages is an FET of a first conductivity type and wherein an FET of the first conductivity type and an FET of a second conductivity type are formed on said semiconductor chip.

11. A high frequency power amplifier having a plurality of amplifying systems, said amplifying system comprising:

an input terminal to which a signal to be amplified is supplied;

an output terminal;

a bias terminal;

a plurality of amplifying stages which are sequentially cascaded between said input terminal and output terminal; and

a bias circuit connected to said bias terminal and each of said amplifying stages to apply a bias potential to said amplifying stage, said amplifying stage including a control terminal for receiving an input signal and said bias potential supplied to the stage and a first terminal for transmitting an output signal of the stage, a first amplifying stage and a second amplifying stage of said amplifying stage being monolithically formed on a single semiconductor chip, a part of bias resistors included in the bias circuits of said first amplifying stage and second amplifying system being monolithically formed on said semiconductor chip, the bias resistance ration of the first amplifying stage of said

amplifying system or the bias resistance ratios of the first amplifying stage and second amplifying stage being adjustable.

12. A high frequency power amplifier according to Claim 11, wherein the bias resistance ratio of the first amplifying stage of said amplifying system or the bias resistance ratios of the first amplifying stage and second amplifying stage are adjusted by selecting connecting positions of electrical connectors that connect the plurality of bias resistors formed on the surface of said semiconductor chip, the choice including no connection with the electrical connectors.

13. A high frequency power amplifier according to Claim 11, wherein a transistor that serves as the final amplifying stage of said amplifying system is any of a Si-MOSFET, SiGe-FET, GaAs-MESFET, HEMT, and hetero-junction type bipolar transistor.

14. A wireless communication apparatus comprising a high frequency power amplifier according to Claim 11.